Microprocessor Supervisory Circuit in 4-Lead SC70

Preliminary Technical Data

ADM6384

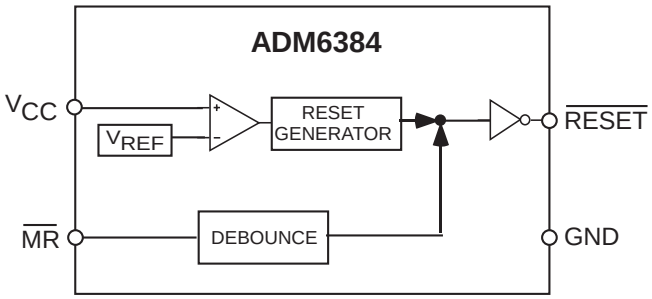
FEATURES

- Precision 1.8V to 5V Power Supply Monitoring
- 31 Reset Threshold Options:
  - 1.58V to 5.0V
- Four Reset Timeouts:
  - 1ms, 20ms, 140ms, 1120ms
- Manual Reset Input
- Reset Output Stage- Push-Pull Active-Low
- Guaranteed Reset Output valid to V_{CC}=1V
- Power Supply Glitch Immunity
- Specified Over -40°C to +125°C Temperature Range
- 4-Lead SC70 Package

APPLICATIONS

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM6384 is a supervisory circuit which monitors power supply voltage levels in microprocessor-based systems. A power-on-reset signal is generated when the supply voltage rises to a preset threshold level. The ADM6384's debounced manual reset input can be used to initiate a reset by means of an external push-button or logic signal.

The part is available in a choice of the following 31 reset threshold options, from 1.58V to 5.0V. The minimum reset timeout periods are 1ms, 20ms, 140ms and 1120ms.

The ADM6384 is available in a 4-lead SC70 package and typically consumes only 7µA, making it suitable for use in low power portable applications

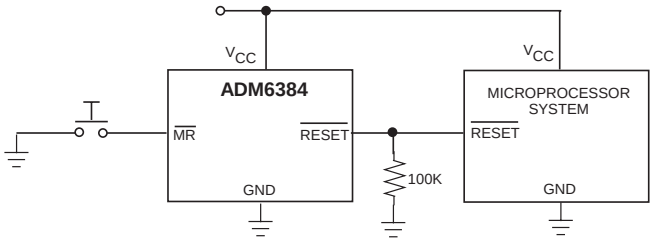


Figure 1. Typical ADM6384 Operating Circuit

Rev. PrD

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ADM6384—SPECIFICATIONS

Table 1. V_{CC}=Full Operating Range, T_A=-40°C to 125°C, unless otherwise noted

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	
Supply Current		7	13	µA	V_{CC}=5.5V, no load
		6	11	µA	V_{CC}=3.6V, no load
		4	7	µA	V_{CC}=2.5V, no load[1]
		3	6	µA	V_{CC}=1.8V, no load[1]
RESET THRESHOLD VOLTAGE					
ADM6384_50_	4.88	5.00	5.12	V	
ADM6384_49_	4.78	4.90	5.02	V	
ADM6384_48_	4.68	4.80	4.92	V	
ADM6384_47_	4.58	4.70	4.82	V	
ADM6384_46_	4.51	4.63	4.74	V	
ADM6384_45_	4.39	4.5	4.61	V	
ADM6384_44_	4.27	4.38	4.48	V	
ADM6384_43_	4.19	4.30	4.41	V	
ADM6384_42_	4.1	4.2	4.31	V	
ADM6384_41_	4.0	4.1	4.2	V	
ADM6384_40_	3.9	4.0	4.1	V	
ADM6384_39_	3.8	3.9	4.0	V	
ADM6384_38_	3.71	3.8	3.9	V	
ADM6384_37_	3.61	3.7	3.79	V	
ADM6384_36_	3.51	3.6	3.69	V	
ADM6384_35_	3.41	3.5	3.59	V	
ADM6384_34_	3.32	3.4	3.49	V	
ADM6384_33_	3.22	3.3	3.38	V	
ADM6384_32_	3.12	3.2	3.28	V	
ADM6384_31_	3.00	3.08	3.15	V	
ADM6384_30_	2.93	3.0	3.08	V	
ADM6384_29_	2.85	2.93	3.00	V	
ADM6384_28_	2.73	2.8	2.87	V	
ADM6384_27_	2.63	2.70	2.77	V	
ADM6384_26_	2.56	2.63	2.69	V	
ADM6384_25_	2.44	2.5	2.56	V	
ADM6384_24_	2.34	2.4	2.46	V	
ADM6384_23_	2.26	2.31	2.37	V	
ADM6384_22_	2.13	2.19	2.24	V	
ADM6384_17_	1.62	1.67	1.71	V	
ADM6384_16_	1.54	1.58	1.61	V	
RESET THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/°C	
RESET THRESHOLD HYSTERESIS		3		mV	
RESET TIMEOUT PERIOD					
ADM6384_ _D1	1		2	ms	
ADM6384_ _D2	20		40	ms	
ADM6384_ _D3	140		280	ms	
ADM6384_ _D4	1120		2240	ms	
VCC to RESET DELAY		35		µs	V_{CC} falling at 10mV/µs
$\overline{\text{RESET}}$ Output Voltage					
VOL			0.3	V	V_{CC}>=1.0V, I_{SINK}=80µA
			0.3	V	V_{CC}>=2.5V, I_{SINK}=1.2mA

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
			0.4	V	V_{CC}>=4.5V, I_{SINK}=3.2mA
VOH	0.8x V_{CC}			V	V_{CC}>=2.5V, I_{SOURCE}=500µA
	0.8x V_{CC}			V	V_{CC}>=4.5V, I_{SOURCE}=800µA
$\overline{RESET}$ Rise Time		5	25	ns	From 10% to 90% V_{CC}, C_L=5pF, V_{CC} =3.3V
MANUAL RESET INPUT					
$\overline{MR}$ Input Threshold					
VIL			0.3xV_{CC}	V	V_{CC} <4V
			0.8	V	V_{CC} <4V
VIH	0.7xV_{CC}			V	V_{CC} >4V
	2.4			V	V_{CC} >4V
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ Pull-up Resistance	32	63	100	kΩ	
$\overline{MR}$ to Reset Delay		200		ns	

[1] T_A = 25°C Only

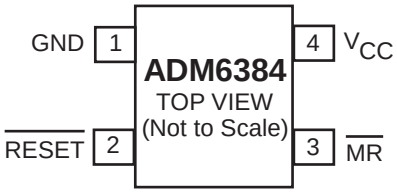
ABSOLUTE MAXIMUM RATINGS

Table 2. T_A = 25°C unless otherwise noted.

Parameter	Rating
V_{CC}	-0.3V to +6V
$\overline{RESET}$	-0.3V to +6V
Output Current ($\overline{RESET}$)	20mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
θ_{JA} Thermal Impedance, SC70	146°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapour Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS AND FUNCTIONAL DESCRIPTIONS



Pin Configuration

Table 3. Pin Functional Descriptions

Pin No.	Name	Description
1	GND	Ground
2	$\overline{\text{RESET}}$	Active-Low Reset Output, which is asserted whenever V_{CC} is below the reset.threshold, V_{TH}. Push-Pull Output Stage.
3	$\overline{\text{MR}}$	Manual Reset Input. This is an active-low input which, when forced low for at least 1µs, generates a reset. Features a 52kΩ internal pull-up.
4	V_{CC}	Power Supply Voltage being Monitored.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

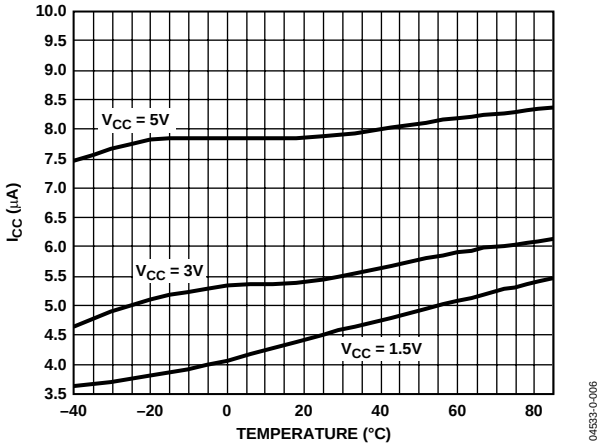


Figure 2. Supply Current vs. Temperature

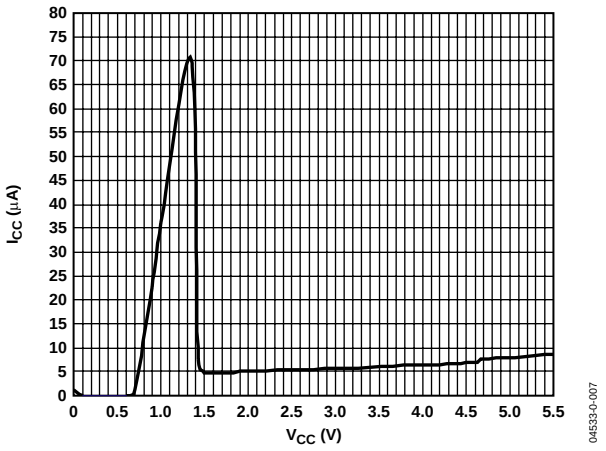


Figure 3. Supply Current vs. Supply Voltage

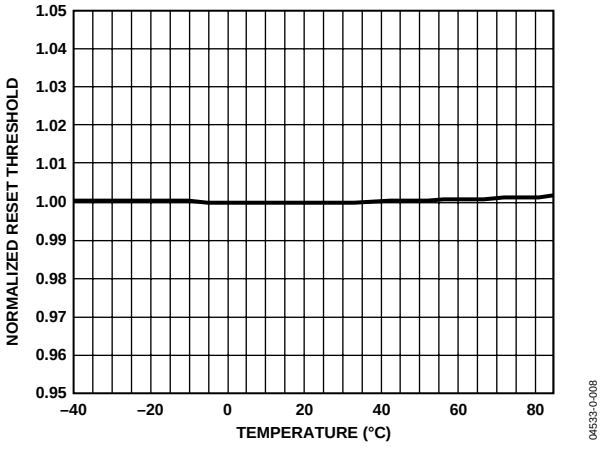


Figure 4. Normalized Reset Threshold vs. Temperature

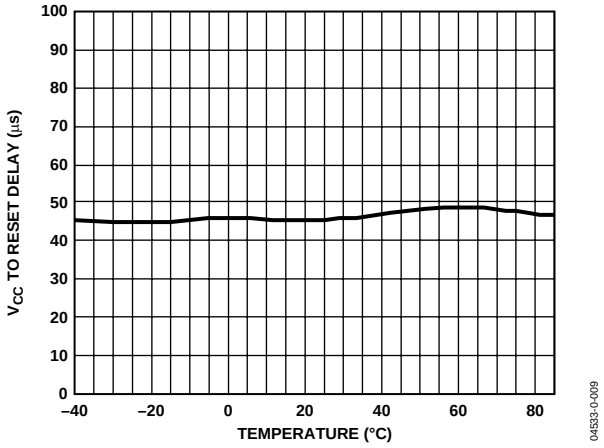


Figure 5. V_{CC} Falling to Reset Propagation Delay vs. Temperature

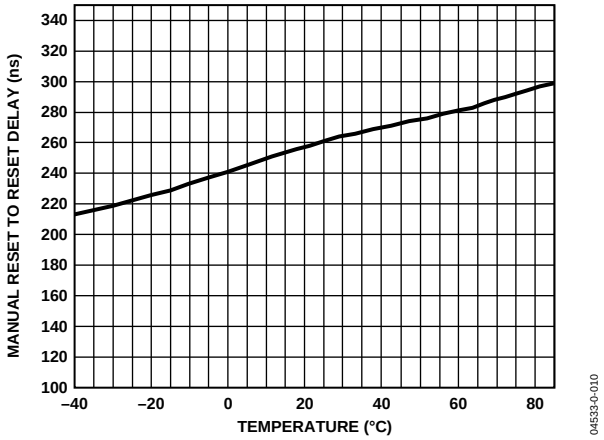


Figure 6. Manual Reset to Reset Propagation Delay vs. Temperature

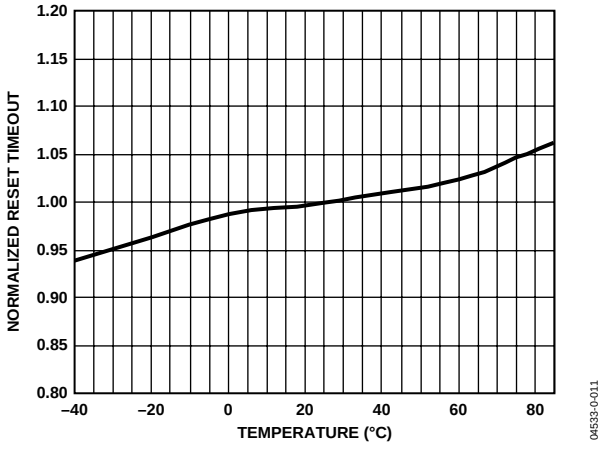


Figure 7. Normalized Reset Timeout Period vs. Temperature

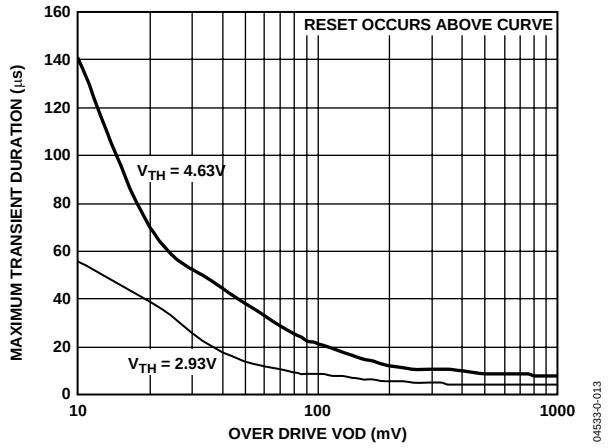


Figure 8. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

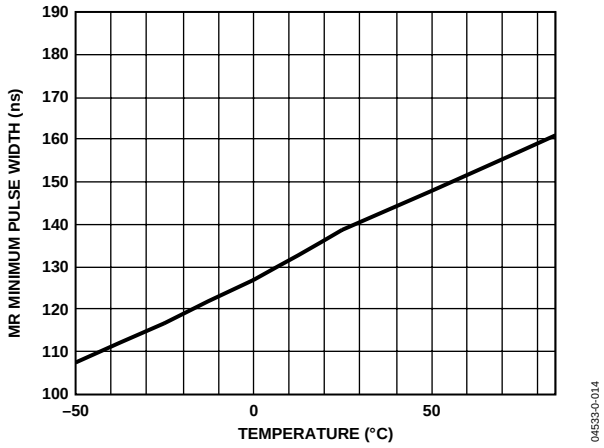


Figure 9. Manual Reset Minimum Pulse Width vs. Temperature

CIRCUIT DESCRIPTION

The ADM6384 provides microprocessor supply voltage supervision by controlling the microprocessor's reset input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed-timeout reset pulse after the supply voltage rises above the threshold. If the user detects a problem with the system's operation, a manual reset input is available to reset the microprocessor by means of an external push-button, for example.

RESET OUTPUT

The ADM6384 features an active-low, push-pull reset output. The reset signal is guaranteed to be logic low for V_{CC} down to 1V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}) or when $\overline{MR}$ is driven low. Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold or after $\overline{MR}$ transitions from low-to-high. Figure 10 illustrates the behavior of the reset outputs.

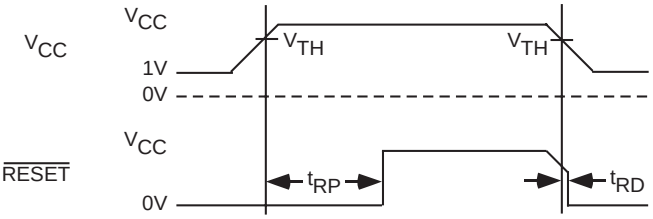


Figure 10. Reset Timing Diagram

MANUAL RESET INPUT

The ADM6384 features a manual reset input ($\overline{MR}$) which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 kΩ internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on-chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients of up to 100 ns (typ) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

APPLICATION INFORMATION

NEGATIVE-GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM6384 is equipped with glitch rejection circuitry. The typical performance characteristic in Figure 8 plots V_{CC} transient duration versus the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 µs typically does not cause a reset, but if the transient is any bigger in magnitude or duration, a reset is generated. An optional 0.1 µF bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC}= 0 V

Both active-low and active-high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active-low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For the active-high case, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. A large resistance such as 100 kΩ should be used so that it does not overload the reset output when V_{CC} is above 1 V.

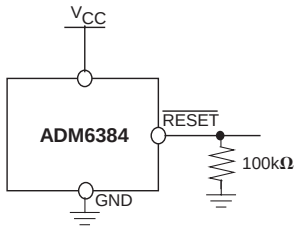


Figure 11. Ensuring Reset Valid to V_{CC} = 0 V

OUTLINE DIMENSIONS

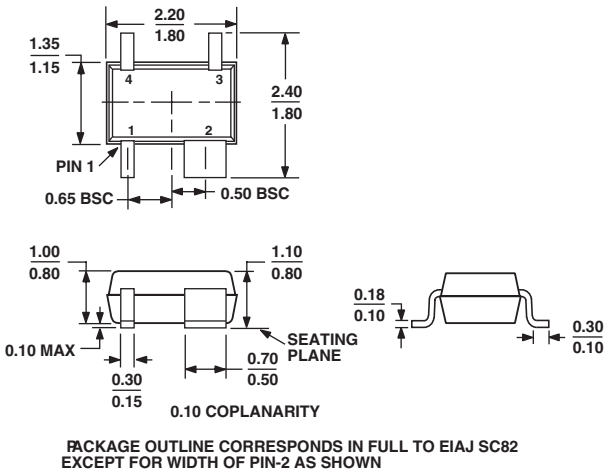


Figure 2. 4-Lead Plastic Surface Mount Package [SC70]

(KS-4)

Dimensions shown in millimeters

ORDERING GUIDE

Table 1. ADM6384 Ordering Guide

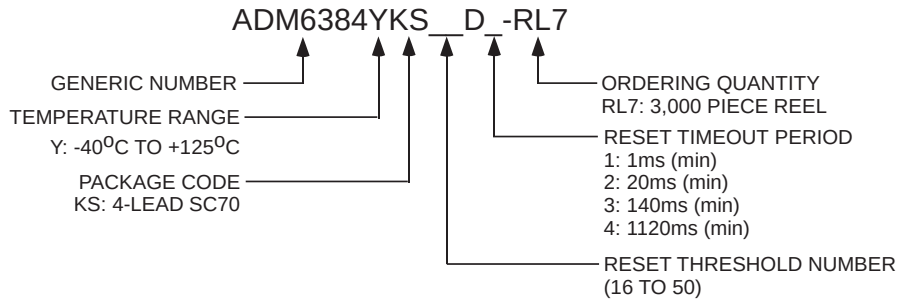


Figure 2. Ordering Code Structure

Model[1,2]	Reset Threshold (V)	Reset Timeout (ms)	Temperature Range	Quantity	Package Type	Branding
ADM6384YKS29D1-R7	2.93	1	–40°C to +125°C	3k	SC70-4	N0J
ADM6384YKS23D3-R7	2.31	140	–40°C to +125°C	3k	SC70-4	N0J
ADM6384YKS26D3-R7	2.63	140	–40°C to +125°C	3k	SC70-4	N0J
ADM6384YKS29D3-R7	2.93	140	–40°C to +125°C	3k	SC70-4	N0J

2

[1] Complete the ordering code by inserting reset timeout, and reset threshold suffixes from Table 1.
[2] Contact Sales for the availability of nonstandard models.